REMARKS/ARGUMENTS

Reconsideration of this application, as amended, is respectfully requested. The following remarks are responsive to the Office Action of October 5, 2004. Claims 6-9 have been cancelled. Claims 21, 22 have been added. Thus, claims 1-5 and 10-22 are presented for examination.

The forgoing amendment and the following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

35 U.S.C. § 102(b) Rejections

Claims 1-5, 10-12, 15, 16, 18 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Noble et al., U.S. Patent No. 5,760,636 (Nobel).

Nobel discloses a method and apparatus for adjusting the clock frequency and voltage supplied to an integrated circuit. First, a signal is sent to the clock, and in response, the clock lowers the clock frequency supplied to the integrated circuit. The clock sends a signal to the voltage regulator whereupon the voltage regulator reduces the voltage supplied to the integrated circuit. (Nobel, Abstract.) Nobel further discloses an embodiment where *execution and operation of the processor within the computer system is **halted during the transitions** from normal operation mode to low power mode and back to normal operation mode.* (Nobel, 5: 41-45.) Because transitions from normal operation mode to low power mode and back to normal operation mode in Nobel comprise modifying ***both*** the clock frequency and the voltage supplied to the integrated circuit (Nobel, 6: 11-15), operation of the processor within the computer system in Nobel is halted while the clock frequency is being modified and also while the voltage supplied to the integrated circuit is being modified. This is in contrast to a component comprising "a clock generator to **switch from a first clock frequency to a second clock frequency while the component is in a sleep state**, the switch from the first to the second clock frequency to be associated with a transition between a high performance state and a low power state; and a core to receive a voltage to **switch from a first voltage level to a second voltage level while the component is in an active mode**, the switch from the first voltage level to the second voltage level to be associated with the transition between the high performance state and the low power state," as recited in claim 1. Because Nobel fails to disclose or suggest each and

every element of claim 1, claim 1 and its dependent claims 2-5 are patentable and should be allowed.

Claim 10 recites "a component to switch its clock frequency from a first clock frequency to a second clock frequency **while the component is in a sleep state** ...; and a voltage regulator to switch a core voltage to the component from a first voltage level to a second voltage level **while the component is in an active mode**." Claims 15 and 18 recite "switching a clock generator of a component from a first clock frequency to a second clock frequency **while the component is in a sleep state** ...; and switching a core voltage from a first voltage level to a second voltage level **while the component is in an active mode**." Thus, claims 10, 15, 18, and their respective dependent claims 11-14 and 16-17, and 19-20 are patentable and should be allowed for at least the reasons articulated with respect to claim 1.

Claims 6, 7 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Gebara et al., U.S. Patent No. 6,035,407. Claims 6, 7 and 9 have been cancelled.

35 U.S.C. § 103(a) Rejections

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gebara et al. U.S. Patent No. 6,035,407. Claim 8 has been cancelled.

Claims 13-14, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nobel et al., U.S. Patent No. 5,760,636, in view of Gebara et al., U.S. Patent No. 6,035,407.

Claims 13-14 require "a component to switch its clock frequency from a first clock frequency to a second clock frequency **while the component is in a sleep state** ...; and a voltage regulator to switch a core voltage to the component from a first voltage level to a second voltage level **while the component is in an active mode**" by virtue of being dependent on claim 10. Claims 17 and 20 recite "switching a clock generator of a component from a first clock frequency to a second clock frequency **while the component is in a sleep state** ...; and switching a core voltage from a first voltage level to a second voltage level **while the component is in an active mode**" by virtue of being dependent on claims 15 and 18 respectively. Nobel, Gebara, and a combination thereof fail to disclose or suggest the above-identified elements. Thus, claims 13-

14, 17 and 20 are patentable and should be allowed for at least the reasons articulated with respect to claim 1.

Conclusion

Having tendered the above remarks and amended the claims as indicated herein, Applicant respectfully submits that all rejections have been addressed and that the claims are now in a condition for allowance, which is earnestly solicited.

If there are any additional charges, please charge Deposit Account No. 02-2666. If a telephone interview would in any way expedite the prosecution of the present application, the Examiner is invited to contact Elena Dreszer at (408) 947-8200 ext. 209.

Respectfully submitted,

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